

PD auto generated file incorrect spelling causes build error. TOPOLOGY\_SIGNLE\_32\_BIT.

D:\intelFPGA\_pro\23.2\ip\altera\intel\_hps\sm\mpfe\intel\_mpfe\_sundancemesa\_hw.tcl lines 58

D:\intelFPGA\_pro\23.2\ip\altera\intel\_hps\sm\mpfe\_lite\intel\_mpfe\_lite\_sundancemesa\_hw.tcl lines 41